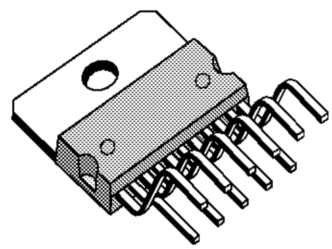
SGS-THOMSON MICROELECTRONICS

TDA1675A

VERTICAL DEFLECTION CIRCUIT

- SYNCHRONISATION CIRCUIT
- ESD PROTECTED
- PRECISION OSCILLATOR AND RAMP GENERATOR
- POWER OUTPUT AMPLIFIER WITH HIGH CURRENT CAPABILITY
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT SCREEN PROTECTION CIRCUIT WHICH BLANKS THE BEAM CURRENT IN THE EVENT OF LOSS OF VERTICAL DEFLECTION CURRENT



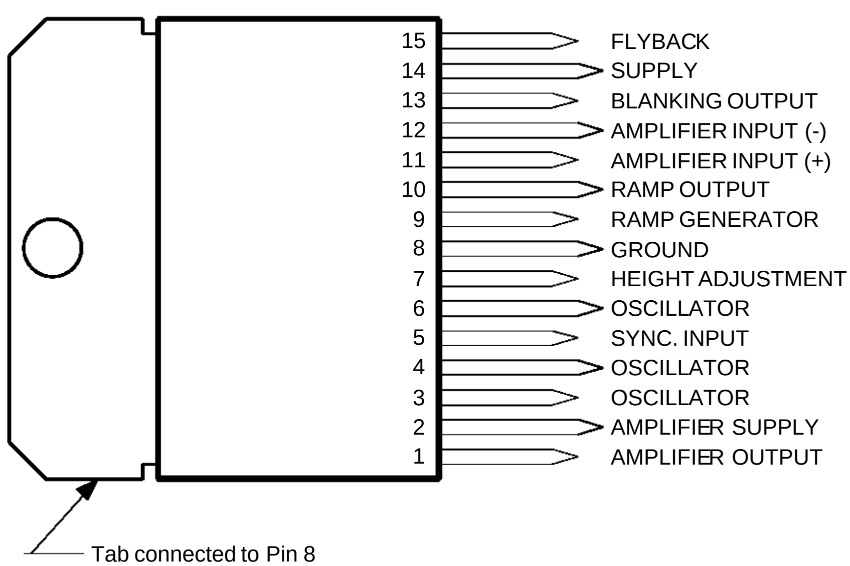
MULTIWATT 15
(Plastic Package)

ORDER CODE : TDA1675A

DESCRIPTION

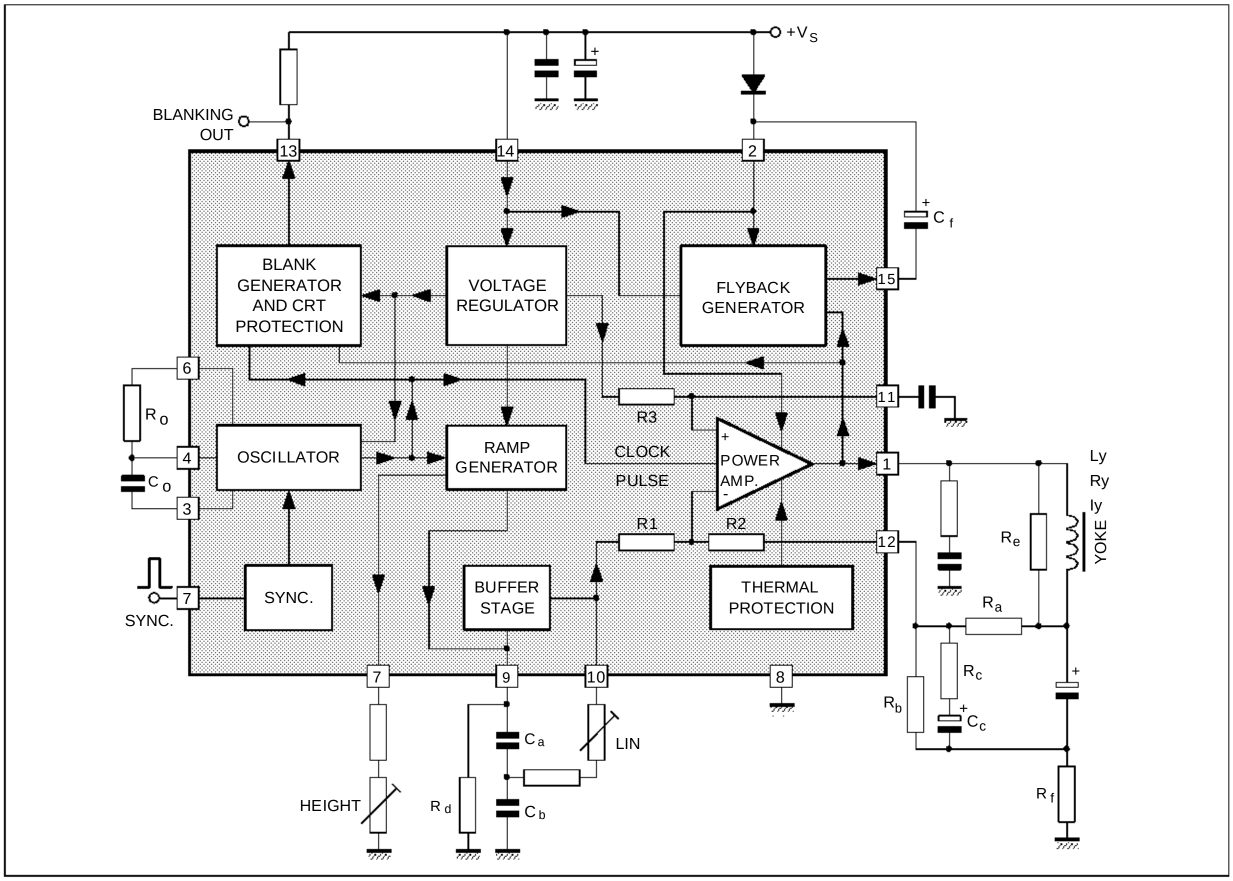
The TDA1675A is a monolithic integrated circuit in 15-lead Multiwatt® package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, B&W TVs, monitors and displays.

PIN CONNECTIONS (top view)



1675A-01.EPS

BLOCK DIAGRAM



1675A-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 14	35	V
V_1, V_2	Flyback Peak Voltage	65	V
V_5	Sync. Input Voltage	20	V
V_{11}, V_{12}	Power Amplifier Input Voltage	V_S - 10	V
V_{13}	Voltage at Pin 13	V_S	
I_O	Output Current (non repetitive) at t = 2ms	3	A
I_O	Output Peak Current at f = 50Hz t > 10µs	2	A
I_O	Output Peak Current at f = 50Hz t ≤ 10 µs	3.5	A
I_{15}	Pin 15 Peak-to-peak Flyback Current at f = 50Hz, tfly ≤ 1.5ms	3	A
I_{15}	Pin 15 D.C. Current at V1 < V_{14}	100	mA
P_{tot}	Maximum Power Dissipation at T_{case} ≤ 60°C	30	W
T_{stg}, T_j	Storage and Junction Temperature	- 40, + 150	°C

1675A-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W
$R_{TH(j-a)}$	Thermal Resistance Junction-ambient	Max.	40	°C/W

1675A-02.TBL

DC ELECTRICAL CHARACTERISTICS (V_S = 35V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 quiescent current	$I_1 = 0$		16	36	mA	1b
$- I_9$	Ramp generator bias current	$V_9 = 0$		0.02	1	µA	1b
$- I_9$	Ramp generator current	$V_9 = 0$; $- I_7 = 20\mu A$	18.5	20	21.5	µA	1b
$\frac{\lvert \Delta I_9 \rvert}{I_9}$	Ramp generator non linearity	ΔV_9 = 0 to 15V, $- I_7 = 20\mu A$		0.2	1	%	1b
I_{14}	Pin 14 quiescent current			25	45	mA	1b
V_1	Quiescent output voltage	$V_S = 35V, R_a = 2.2k\Omega, R_b = 1k\Omega$ $V_S = 15V, R_a = 390\Omega, R_b = 1k\Omega$	16.4 6.9	17.8 7.5	19.5 8.1	V V	1a
V_{1L}	Output saturation voltage to ground	$I_1 = 1.2A$,		1	1.4	V	1c
V_{1H}	Output saturation voltage to supply	$- I_1 = 1.2A$		1.6	2.2	V	1d
V_4	Oscillator virtual ground			0.45		V	1b
V_7	Regulated voltage at pin 7	$- I_7 = 20\mu A$	6.3	6.6	7	V	1b
$\frac{\Delta V_7}{\Delta V_S}$	Regulated voltage drift with supply voltage	ΔV_S = 15 to 35V		1	2	$\frac{mV}{V}$	1b
V_{11}	Amplifier input (+) reference voltage		4.1	4.4	4.7	V	1b
V_{13}	Blanking output saturation voltage	I_{13} = 10 mA		0.35	0.5	V	1a
V_{15}	Pin 15 saturation voltage to ground	I_{15} = 20 mA		1	1.5	V	1a

1675A-03.TBL

Figure 1 : DC Test Circuit.

Figure 1a

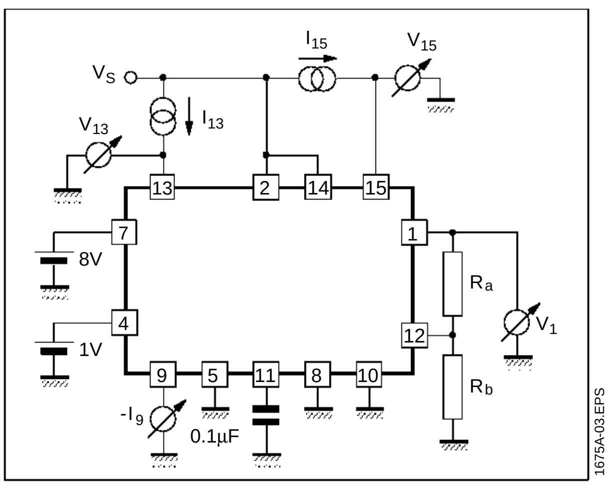


Figure 1b

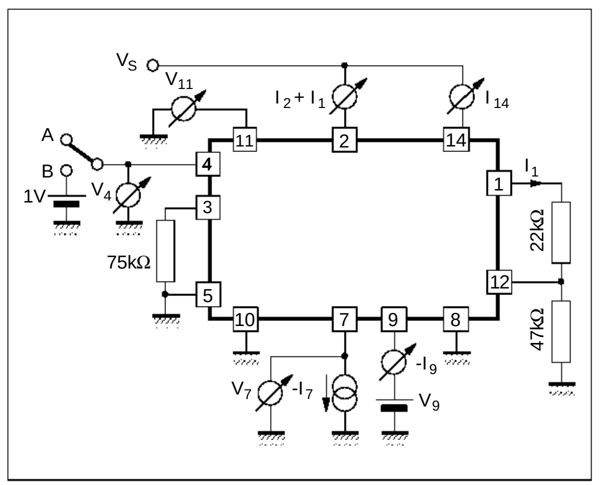


Figure 1c

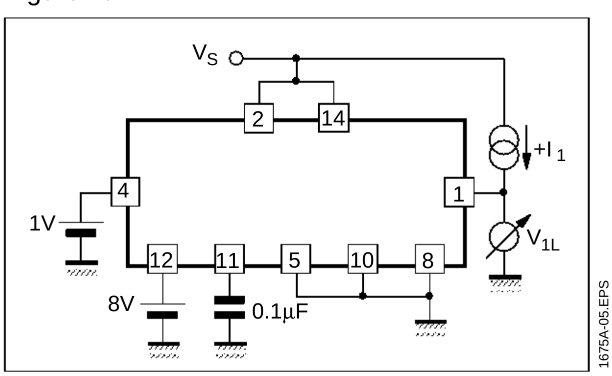
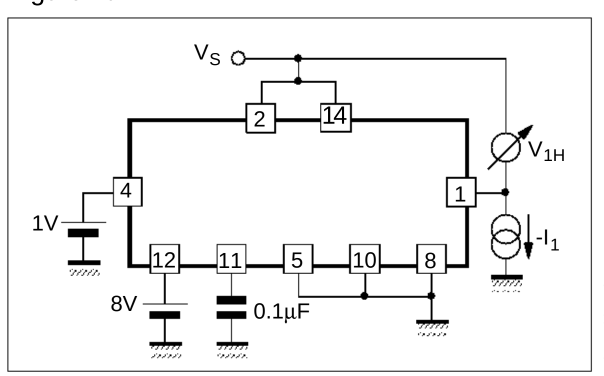


Figure 1d



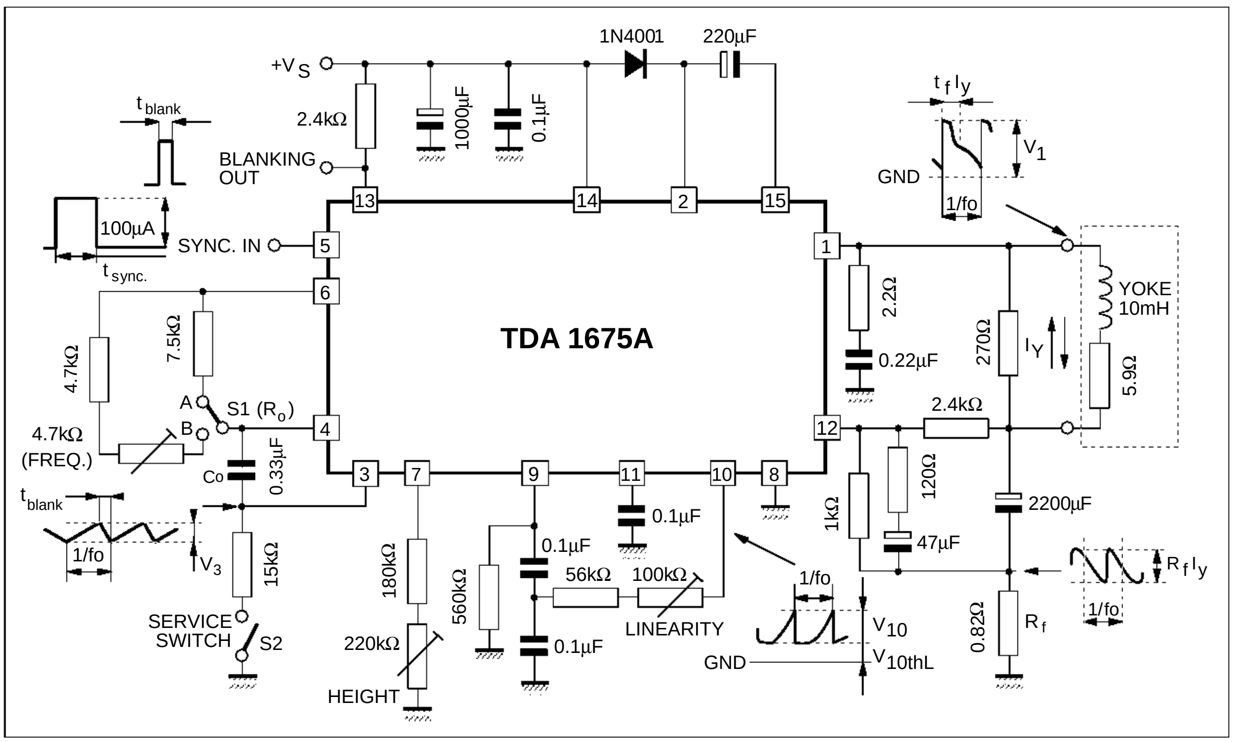
AC ELECTRICAL CHARACTERISTICS

(Refer to A.C. test circuit of fig. 2, T_{amb} = 25°C, V_S = 24V, f = 50Hz, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	I_Y = 2A_{PP}		295		mA
I_5	Sync Input Current Required to Sync		100			µA
V_1	Flyback Voltage	I_y = 2App		50		V
V_3	Peak-to-peak Oscillator Sawtooth Voltage	I_5 = 0 I_5 = 100µA		3.6 3.4		V V
$V_{10TH(L)}$	Start Scan Level of the Input Ramp			1.85		V
t_{FLY}	Flyback Time	Iy = 2App		0.6		ms
t_{BLANK}	Blanking Pulse Duration	f_o = 50Hz, T_j = 75°C f_o = 60Hz, T_j = 75°C	1.33	1.4 1.17	1.47	ms ms
f_o	Free Running Frequency	R_o = 7.5kΩ, C_o = 330nF, T_j = 75°C R_o = 6.2kΩ, C_o = 330nF, T_j = 75°C	42	43.5 52.5	46	Hz Hz
Δf	Synchronization Range	I_5 = 100µA, T_j = 75°C	14	16		Hz
T_j	Junction Temperature for Thermal Shut-down			145		°C
V_{ON}	Peak-to-peak Output Noise				35	mV_{PP}

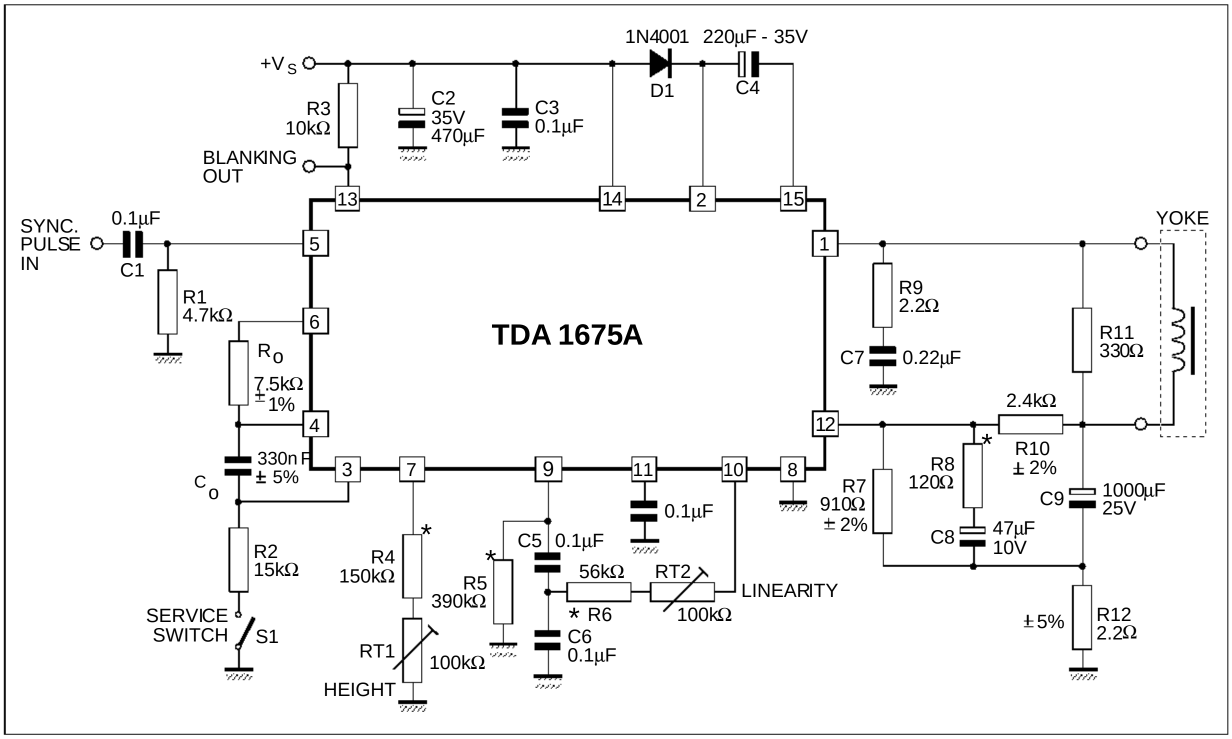
1675A-04.TBL

Figure 2 : AC Test Circuit



1675A-07.EPS

Figure 3 : Application Circuit for Small Scree 90° CTV Set (R_y = 15Ω ; L_y = 30 mH ; I_y = 0.82 A_{PP})



* The value depends on the characteristics of the CRT. The value shown is indicative only.

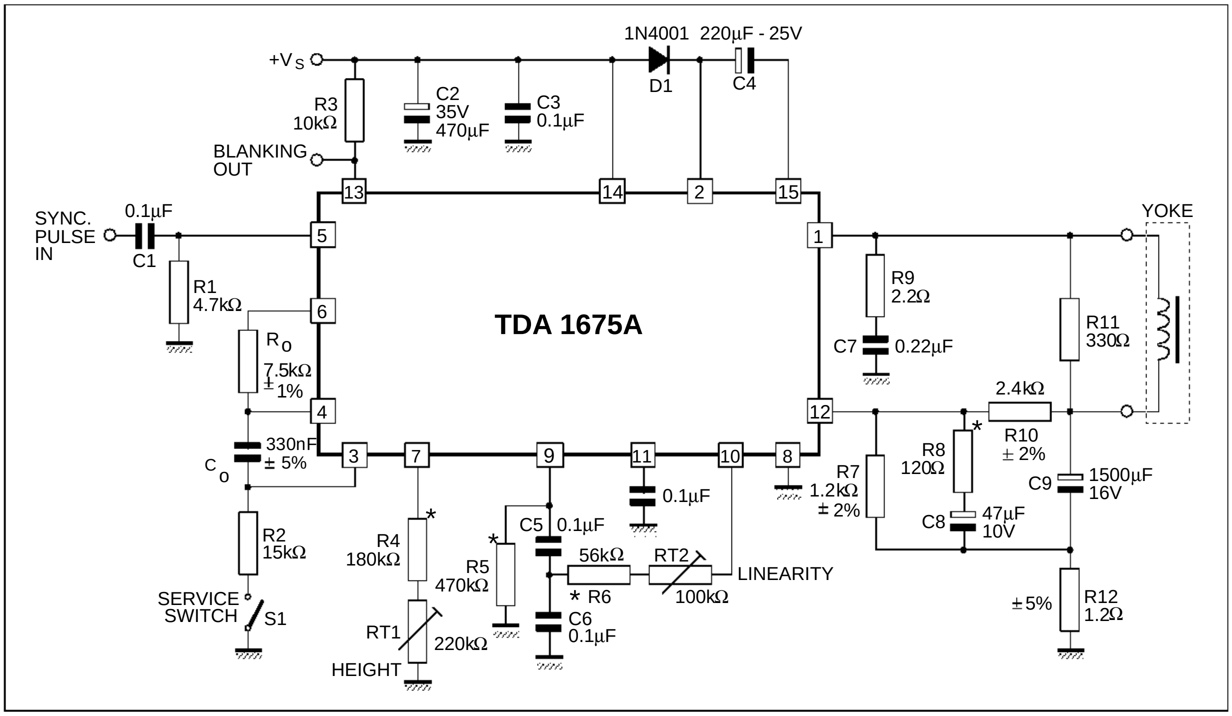
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	25	V
I_S	Supply current	140	mA
t_{FLY}	Flyback time	0.7	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	2.4	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for T_{amb} = 60°C and $T_{j\ max}$ = 110°C for T_{amb} = 60°C and $T_{j\ max}$ = 120°C	 13 16	 °C/W °C/W

1675A-05.TBL

* Worst case condition.

Figure 4 : Application Circuit for 110^o CTV Set (R_y = 9.6Ω ; L_y = 24.6 mH ; I_y = 1.2 A_{PP})



1675A-09.EPS

* The value depends on the characteristics of the CRT. The value shown is indicative only.

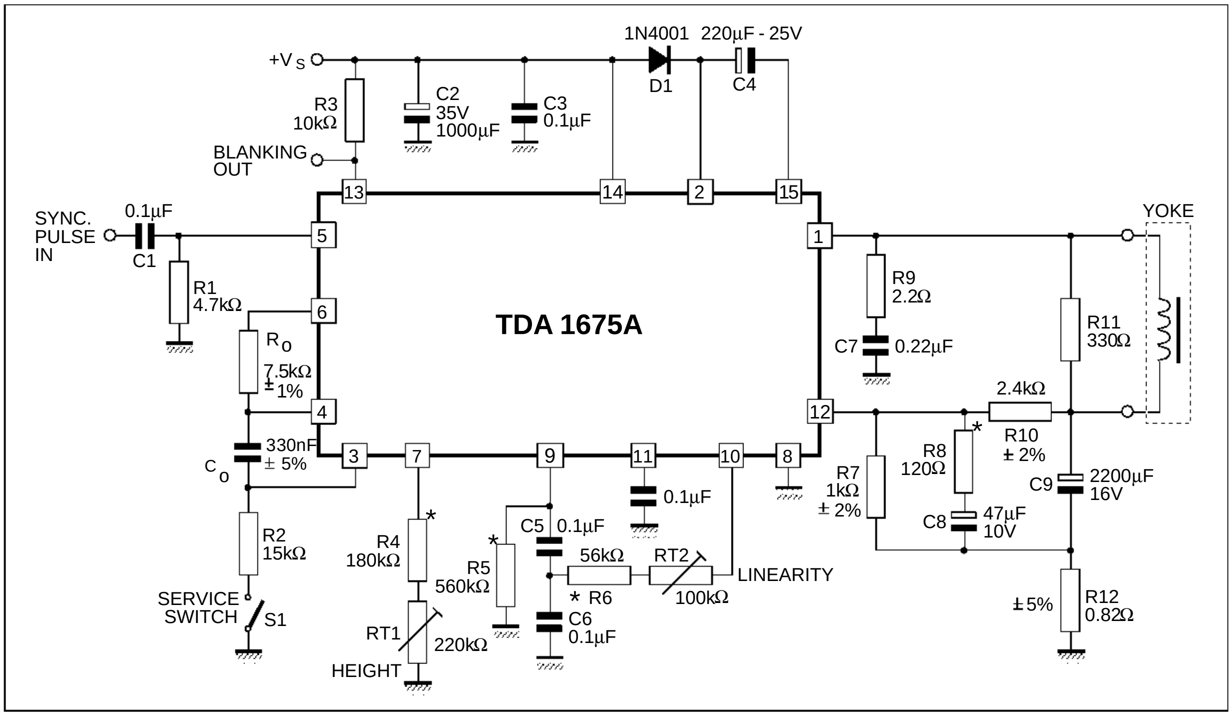
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	22.5	V
I_S	Supply current	185	mA
t_{FLY}	Flyback time	1	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	2.7	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for Tamb = 60^oC and $T_{j\ max}$ = 110^oC for T_{amb} = 60^oC and $T_{j\ max}$ = 120^oC	 11.5 14.5	 $^oC/W$ $^oC/W$

1675A-06.TBL

* Worst case condition.

Figure 5 : Application Circuit for 110° CTV Set (R_y = 5.9Ω ; L_y = 10 mH ; I_y = 1.95 A_{PP})



1675A-10.EPS

* The value depends on the characteristics of the CRT. The value shown is indicative only.

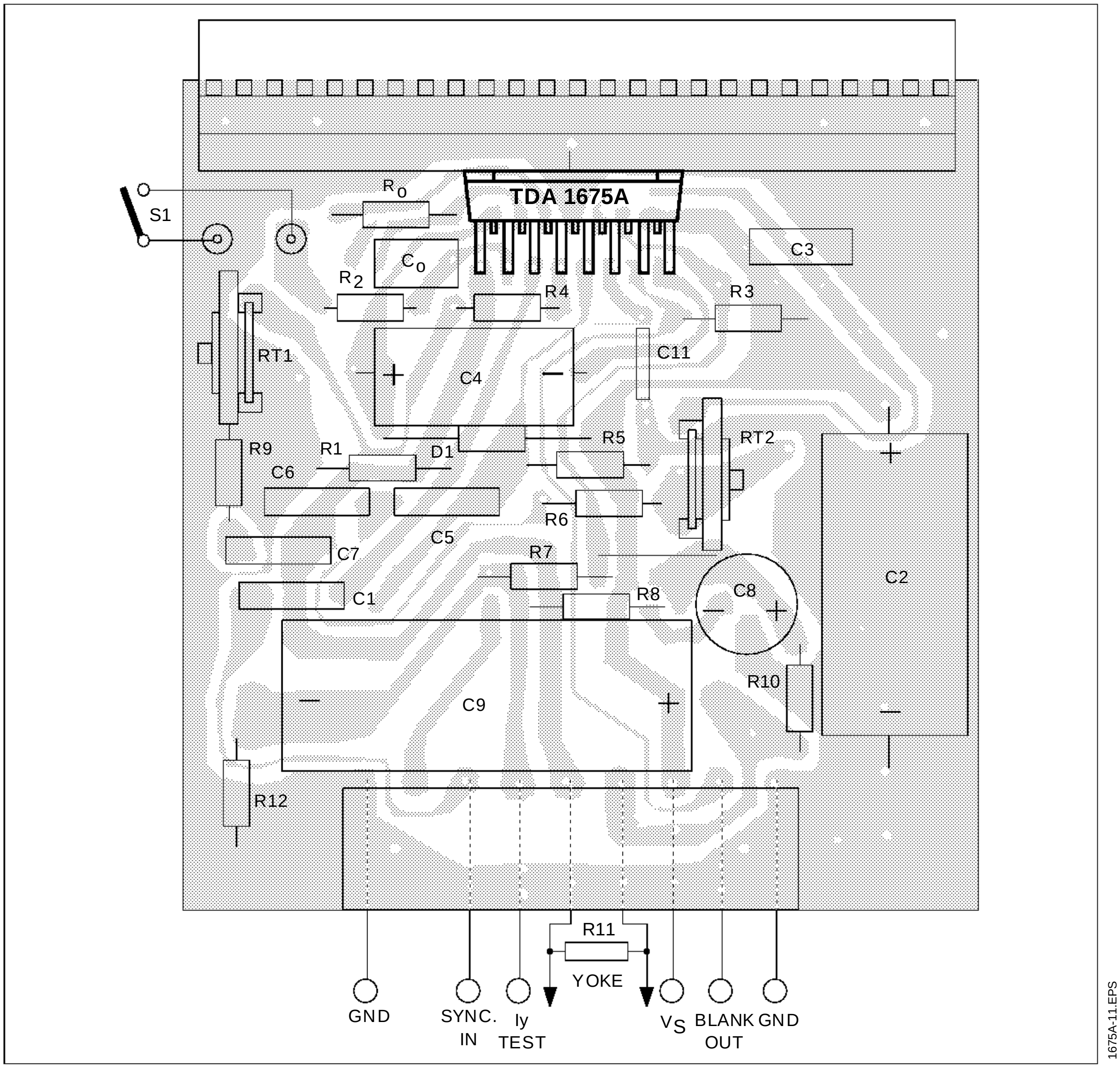
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	24	V
I_S	Supply current	285	mA
t_{FLY}	Flyback time	0.6	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	4.3	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for Tamb = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 6.5 8.5	 °C/W °C/W

1675A-07.TBL

* Worst case condition.

Figure 6 : PC Board and Components Layout for the Application Circuits of Figures 3, 4 and 5 (1 : 1 scale)



APPLICATION INFORMATION (Refer to the block diagram)

Oscillator and sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches R_o high or low so allowing the charge or the discharge of C_o under constant current conditions.

The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 4 is the inverting input of the amplifier used as integrator.

Pin 6 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

Pin 3 is the output of the amplifier.

Pin 5 is the input for sync pulses (positive)

Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor a new voltage ramp is immediately allowed.

The required value of the capacitance is obtained by means of the series of two capacitors Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from C_a and C_b.

Pin 7 The resistance between pin 7 and ground defines the current mirror current and than the height of the scanning.

Pin 9 is the output of the current mirror that charges the series of C_a and C_b. This pin is also the input of the buffer stage.

Pin 10 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.

The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.

The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 12 is the inverting input of the amplifier. An external network, R_a and R_b, defines the DClevel across C_y so allowing a correct centering of the output voltage. The series network R_c and C_c, in conjunction with R_a and R_b, applies at the feedback input I_2 a small part of the parabola, available across C_y, and AC feedback voltage, taken across R_f. The external components R_c, R_a and R_d, produce the linearity correction on the output scanning currently and their values must be optimized for each type of CRT.

Pin 11 is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured. A capacitor must be connected to increase the performances from the noise point of view.

Pin 1 is the output of the power amplifier and it drives the yoke by a negative slope current ramply. R_e and the Boucherot cell are used to stabilize the power amplifier.

Pin 2 The supply of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_S by a diode, while during the retrace time this pin is supplied from the flyback generator.

Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).

The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 14, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.

An integrated diode stops the rising of this output increase and the voltage jump is transferred by means of capacitor C_f at the supply voltage pin of the power stage (pin 2).

When the current across the yoke changes its direction, the output of the flyback generator falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power output amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.

Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 1) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 15 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor C_f transfers the jump to pin 2 (see pin 2).

Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time

when a flyback pulse has been generated. If the flyback pulse is absent (short cirucit or open cirucit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 13 is an open collector output where the blanking pulse is available.

Voltage regulator

The main supply voltage V_S, is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 14 is the main supply voltage input V_S (positive).

Pin 8 is the GND pin or the negative input of V_S

Figure 7 : Output Saturation Voltage to Ground vs. Peak Output Current

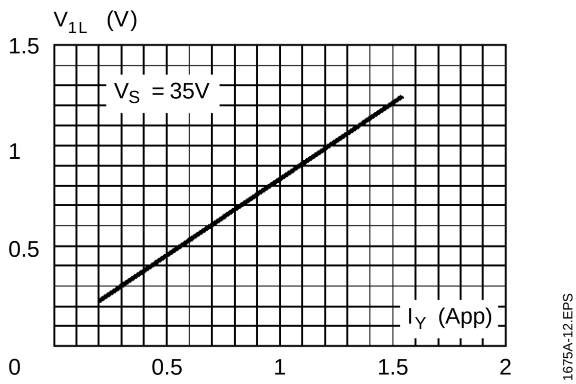


Figure 8 : Output Saturation Voltage to Supply versus Output Peak Current

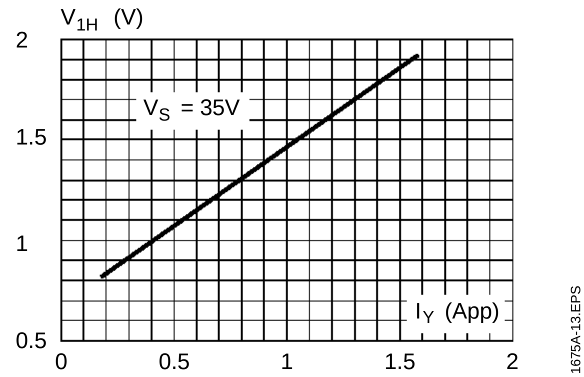
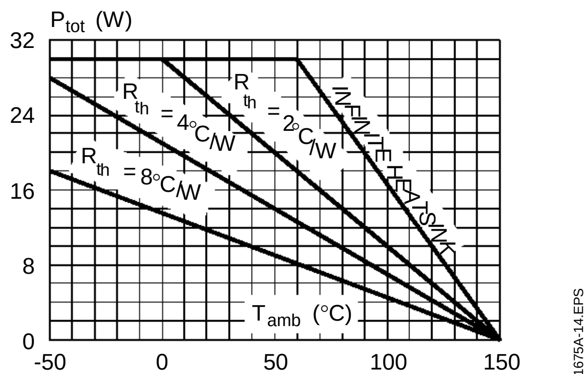


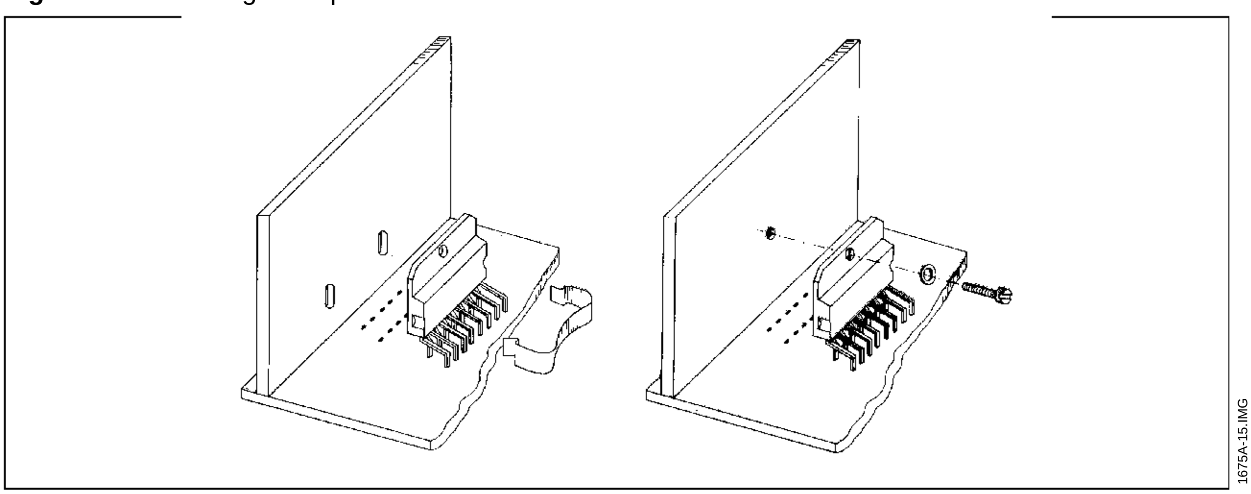
Figure 9 : Maximum allowable Power Dissipation vs. Ambient Temperature



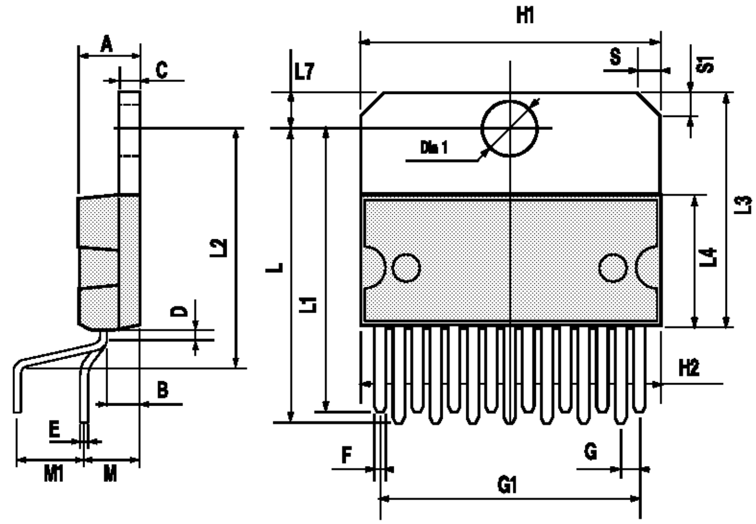
MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the MULTIWATT ® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package, it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Figure 10 : Mounting Examples



PACKAGE MECHANICAL DATA : 15 PINS - PLASTIC MULTIWATT



PMMUL15V.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia. 1	3.65		3.85	0.144		0.152

MUL15V.TBL

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